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ISL54227IRTZEVAL1Z Evaluation Board User Manual

Description

The ISL54227IRTZEVAL1Z evaluation board is designed to provide a quick and easy method for evaluating the ISL54227 USB Switch IC.

The ISL54227 device is a unique IC. To use this evaluation board properly, requires a thorough knowledge of the operation of the IC. See the ISL54227 datasheet for an understanding of the functions and features of the device. Studying the device's truth-table along with its pinout diagram on page 2 of the datasheet is the best way to get a quick understanding of how the part works.

A picture of the evaluation board is shown in Figure 1. The ISL54227 TDFN IC is soldered onto the evaluation board. It is located in the center of the board and is designated as U1.

The evaluation board contains USB connectors, banana jacks, and toggle switches, to allow the user to easily interface with the IC to evaluate its functions, features, and performance. For example, with the board properly powered and configured as shown in Figure 2 you can control the logic pins with the toggle switches, S1 (LP) and S2 (OE), to connect and disconnect the USB device from the USB host (computer).

In a typical application, the ISL54227 dual SPST part is used for switching or isolating a USB source in portable powered products.

This application note will guide the user through configuring and using the evaluation board to evaluate the ISL54227 device.

Evaluation Board Photo

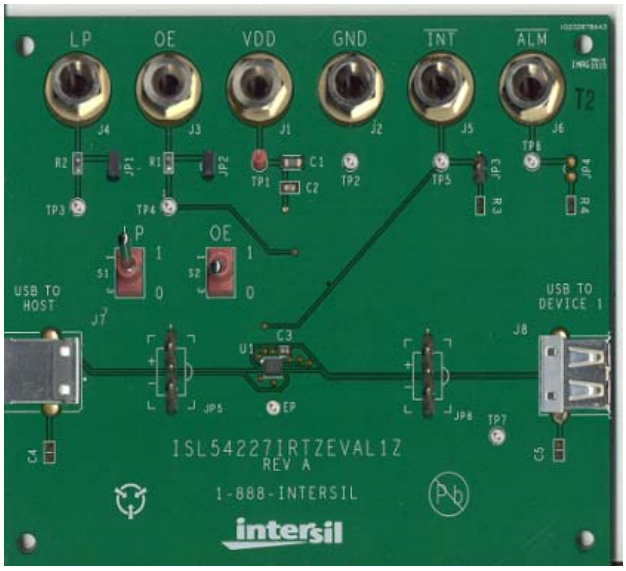

FIGURE 1. ISL54227IRTZEVAL1Z (REV A) EVALUATION BOARD

Key Features

- Standard USB Connectors
- Banana Jacks for Power, Ground and Logic Input and Output Connections
- Toggle Switches for Easy Control of the Logic Pins
- Convenient Test Points and Connections for Test Equipment

Board Architecture/Layout

Basic Layout of Evaluation Board

The basic layout of the evaluation board is as follows: Refer to Figure 1 or the "ISL54227IRTZEVAL1Z Board Schematic" on page 4.

- Power and Ground connections are at banana jacks (J1 and J2) located at the top of the board.
- Logic input connections, OE and LP, are at banana jacks (J3 and J4) located at the top left side of the board or by using the toggle switches S1 and S2. Jumpers JP1 and JP2 must be installed to use the toggle switches. To control the logic through the banana jacks (J3 and J4) the JP1 and JP2 jumpers must not be populated.
- Logic output connections, $\overline{INT}$ and $\overline{ALM}$, are at the top right side of the board at banana jacks (J5 and J6).
- USB connection to an upstream host controller (Computer) is made at the USB connector J7, located at the left side of the board.
- USB connection to the downstream USB device is made at USB connector J8, located on right side of the board.
- The ISL54227 IC (U1) is located in the center of the board. The evaluation board has a Pin 1 indicator dot to show how the IC should be oriented on the evaluation board. The IC Pin 1 indicator dot should be aligned with the evaluation board Pin 1 indicator dot.

IC Power Supply

A DC power supply connected at banana jacks J1 (VDD) and J2 (GND) provides power to the ISL54227 IC. The IC requires a 2.7VDC to 5.25VDC power supply for proper operation. The power supply should be capable of delivering 500µA of current.

Logic Control

The state of the ISL54227 device is determined by the voltage at the LP pin and the OE pin. Access to the LP pin is through the banana jack J4 (LP) or the toggle switch S1 (LP). Access to the OE pin is through the banana jack J3 (OE) or the toggle switch S2 (OE). To use the toggle switches to control the logic, jumpers must be installed at JP1 and JP2. Remove jumpers to control the logic through the banana jacks.

If OE is driven “HIGH” (pulled up to VDD) and LP = “LOW” (to ground) with the signal voltage in the range of 0V to 3.6V, the SPST switches will be ON. The USB host controller (computer) connected at J7 will be connected through to the USB device connected at J8 and data will be transmitted between the computer and the device.

If OE is driven “LOW” (to ground) and LP = “LOW” (to ground) with the signal voltage in the range of 0V to 3.6V, the SPST switches will be OFF. The USB host controller (computer) connected at J7 (USB TO HOST) will be disconnected from the USB device connected at J8 (USB TO DEVICE) and no data will be transferred.

If OE = “LOW” and LP = “HIGH” the switches will be OFF and the part will be put in the low power state. In the low power state the part draws only 5µA (typ) of I_{DD} current.

If the signal at the host (computer side) of the switch is >3.8V (typ) or ≤0.45V (typ) the ISL54227 IC will turn the switches OFF and internally pull the $\overline{ALM}$ pin “LOW”.

$\overline{INT}$ and $\overline{ALM}$ OUTPUT

Access to the ISL54227 $\overline{INT}$ pin is at banana jack J5 ($\overline{INT}$). During normal USB transmission or an overvoltage (OVP) condition this pin outputs a “HIGH”. The ISL54227 part internally pulls this pin “LOW” when the COM pins have been tied together and the OE pin is “LOW”. The purpose of the pin is to be monitored by a µP to tell when a charger has been connected into the USB port. See the ISL54227 datasheet page 10 for description of “Charger Port Detection”.

Access to the ISL54227 $\overline{ALM}$ pin is at banana jack J6 ($\overline{ALM}$). During normal USB transmission this pin will output a “HIGH”. The $\overline{ALM}$ pin gets internally pulled “LOW” whenever the part senses an overvoltage condition. It can be monitored by a µP for the “LOW” state to determine when an overvoltage condition has occurred.

USB Connections

A “B” type USB receptacle labeled “USB TO HOST” (J7) is located at the right side of the board. This receptacle should be connected, using a standard USB cable, to the upstream USB host controller, which is usually a PC computer or hub.

An “A” type USB receptacle labeled “USB TO DEVICE” (J8) is located on the right side of the board. A USB device can be plugged directly into this receptacle or through a standard USB cable.

The USB switches are bi-directional, which allows the host (computer) and downstream USB device to both send and receive data.

High-Speed Switches

The two SPST switches are bi-directional switches that can pass signals up to 3.6V with a V_{DD} supply voltage in the range of 2.7V to 5.25V.

When powered with a 2.7V supply, these switches have a nominal r_{ON} of 3.5Ω over the signal range of 0V to 400mV with a r_{ON} flatness of 0.26Ω. The r_{ON} matching between the SPST switches over this signal range is only 0.2Ω ensuring minimal impact by the switches to USB high-speed signal transitions. As the signal level increases, the r_{ON} switch resistance increases. At signal level of 3.3V the switch resistance is nominally 6.8Ω.

The SPST switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals typically in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high-speed signal quality specifications.

The SPST switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling.

The maximum normal operating signal range for the SPST switches is from 0V to 3.6V. For normal operation, the signal voltage should not be allowed to exceed this voltage range or go below ground by more than -0.3V.

However, in the event that a positive voltage >3.8V (typ) to 5.25V, such as the USB 5V, the V_{BUS} voltage, gets shorted to one or both of the COM+ and COM- pins or a negative voltage ≤0.5V (typ) to -5V gets shorted to one or both of the COM pins, the ISL54227 has OVP circuitry to detect the overvoltage condition and open the SPST switches to prevent damage to the USB down-stream transceiver connected at the signal pins (D+ and D-).

The OVP and power-off protection circuitry allows the COM pins (COM-, COM+) to be driven up to 5.25V while the V_{DD} supply voltage is in the range of 0V to 5.25V. In this condition the part draws <100µA of I_{COMx} and I_{DD} current and causes no stress to the IC. In addition, the SPST switches are OFF and the fault voltage is isolated from the other side of the switch.

The $\overline{ALM}$ pin gets internally pulled “LOW” whenever the part senses an overvoltage condition. It can be monitored by a µP for the “LOW” state to determine when an overvoltage condition has occurred.

Board Component Definitions

Evaluation board components and their functions are shown in Table 1.

TABLE 1. BOARD COMPONENT DESCRIPTIONS

DESIGNATOR	DESCRIPTION
U1	ISL54227IRTZ IC
J7	“B” type USB Receptacle
J8	“A” type USB Receptacle
J1	VDD Positive Connection
J2	VDD Negative Connection
J3	OE Logic Control
J4	LP Logic Control
J5	$\overline{INT}$ Logic Output
J6	$\overline{ALM}$ Logic Output
S1	LP Toggle Switch
S2	OE Toggle Switch
JP5, JP6	D-/D+ Differential Probe Connection
JP1	Toggle Switch S1 (LP) Jumper
JP2	Toggle Switch S2 (OE) Jumper
JP3	$\overline{INT}$ Output Load Jumper
JP4	$\overline{ALM}$ Output Load Jumper

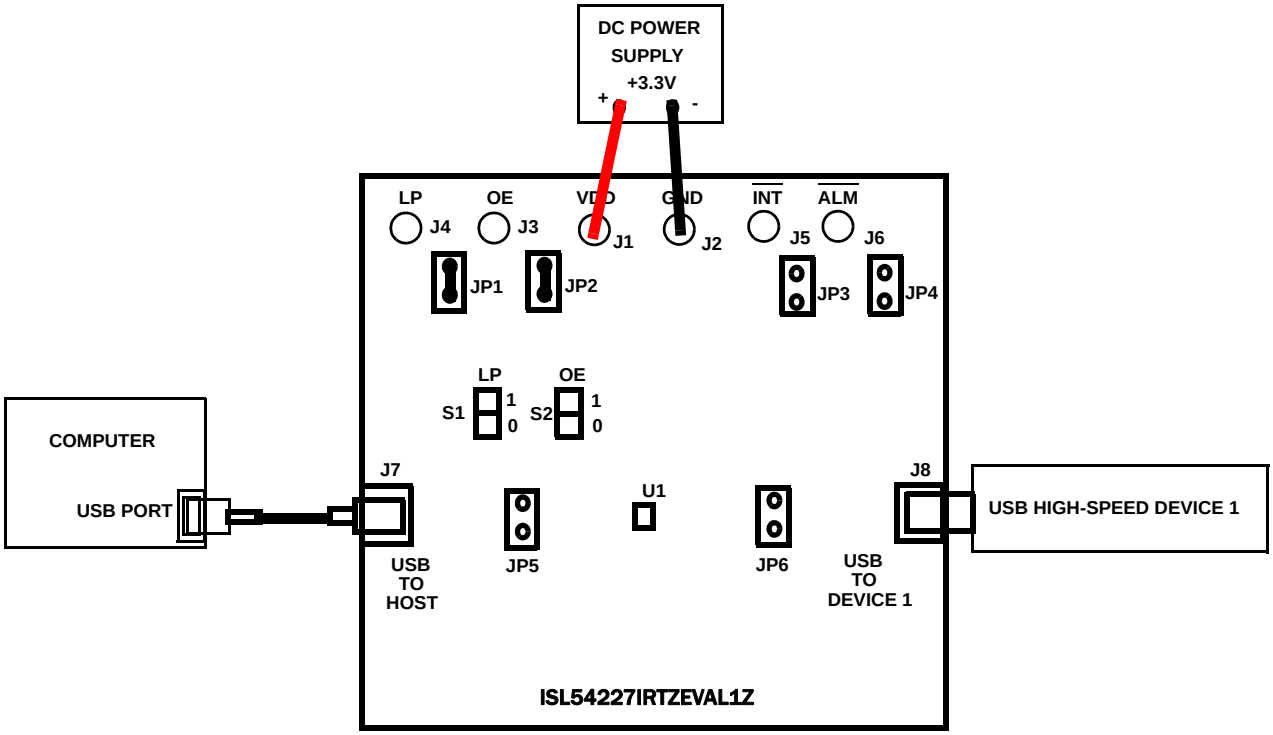

FIGURE 2. BASIC EVALUATION TEST SETUP BLOCK DIAGRAM

Using the ISL54227IRTZEVAL1Z Evaluation Board (see Figure 2)

Lab Equipment

The equipment, external supplies and signal sources needed to operate the board are listed as follow:

1. +2.7V to +5.25V DC Power Supply
2. One High-Speed USB device (i.e. USB memory stick, MP3 Player, etc.)
3. Computer with 2.0 High-Speed USB Port
4. Standard USB Cable

Initial Board Setup Procedure

1. Install jumpers at JP1 and JP2. Allows logic control from S1 and S2 toggle switches.
2. Attach the main evaluation board to a DC power supply at J1 (VDD) and J2 (GND). Positive terminal at J1 and negative terminal at J2. The supply should be capable of delivering 2.7V to 5.25V and 500µA of current. Set the supply voltage to 3.3V.
3. Connect the high-speed USB device at USB connector J8. This connector is located on the right side of the evaluation board.
4. Drive the LP control pin LOW by putting toggle switch S1 (LP) in the down position.
5. Drive the OE control pin LOW to open the SPST switches of the ISL54227 IC by putting toggle switch S2 (OE) in the down position.
6. Connect USB cable from host (PC computer) to the USB “B” type receptacle, J7 (USB TO HOST).

High-Speed Operation

1. Apply a logic LOW to the LP pin by putting toggle switch S1 (LP) in the down position.
2. Apply a logic HIGH to the OE pin by putting toggle switch S2 (OE) in the up position.
3. You should now be able to send and receive data between the computer and the USB device connected at J8.
4. To disconnect the USB device from the computer take the OE pin LOW by putting toggle switch S2 (OE) in the down position.

Low Power Operation

1. Apply a logic LOW to the OE pin by putting toggle switch S2 (OE) in the down position.
2. Apply a logic HIGH to the LP pin by putting toggle switch S2 (LP) in the up position.
3. The part will now be in the low power state. The I_{DD} current will drop from 23µA (typ) to 5µA (typ).

Test Points

The board has various test points to allow the user to connect probes to make measurements. The test points are described in Table 2.

TABLE 2.

DESIGNATOR	DESCRIPTION
TP1	V_{DD} test point
TP2	Ground Test Point
TP3	LP Test Point
TP4	OE Test Point
TP5	$\overline{INT}$ Test Point
TP6	$\overline{ALM}$ Test Point

TABLE 2. (Continued)

DESIGNATOR	DESCRIPTION
JP5	D-/D+ Differential Probe Connection - COM Side of Switch
JP6	D-/D+ Differential Probe Connection - USB Device Side of Switch
JP7	VBUS Test Point

You can observe the D- and D+ USB signal at the device side of the switch on an oscilloscope or other test equipment by connecting a differential probe at JP6.

You can observe the D- and D+ USB signal at the COM side of the switch on an oscilloscope or other test equipment by connecting a differential probe at JP5.

ISL54227IRTZEVAL1Z Board Schematic